1. A method comprising:

determining whether a register has been updated; and

if the register is updated, setting an indicator bit.

2. The method of claim 1 including determining whether the register has been updated by checking an indicator bit.

3. The method of claim 2 wherein if the register has not been updated, refraining from transferring the contents of the register back to a memory.

4. The method of claim 2 including determining whether the register has been updated and if so, saving the contents of the register to memory.

5. The method of claim 4 including saving the register contents to memory on a context change.

6. The method of claim 1 including assigning a single indicator bit to a plurality of registers.

7. An article comprising a medium storing instructions that enable a processor-based system to:

determine whether a register has been updated; and

if the register is updated, set an indicator bit.

8. The article of claim 7 further storing instructions that enable the processor-based system to determine whether the register has been updated by checking an indicator bit.

9. The article of claim 8 further storing instructions that enable the processor-based system to refrain from transferring the contents of the register back to a memory if the register has not been updated.

10. The article of claim 8 further storing instructions that enable the processor-based system to determine whether the register has been updated and if so, save the contents of the register to memory.

11. The article of claim 10 further storing instructions that enable the processor-based system to save the register contents to memory on a context change.

12. The article of claim 10 further storing instructions that enable the processor-based system to save

the contents of a plurality of registers to memory if an indicator bit is set.

13. A processor comprising:

a register; and

a storage storing instructions to determine whether a register has been updated and if the register is updated, set an indicator bit.

14. The processor of claim 13 wherein said storage stores instructions that enable the processor to determine whether the register has been updated by checking an indicator bit.

15. The processor of claim 14 wherein said storage stores instructions that enable the processor to refrain from transferring the contents of the register back to a memory.

16. The processor of claim 14 wherein said storage stores instructions that enable the processor to determine whether the register has been updated and if so, save the contents of the register to memory.

17. The processor of claim 16 wherein said storage stores instructions that enable the processor to save the register contents to memory on a context change.

18. The processor of claim 13 including a storage to store said bit.

19. A system comprising:

a processor;

a register coupled to said processor; and

a storage storing instructions to determine whether a register has been updated and if the register is updated, set an indicator bit.

20. The system of claim 19 including a memory and an interface between said memory and said processor.

21. The system of claim 20 wherein said storage stores instructions that enable the processor to determine whether the register has been updated by checking an indicator bit.

22. The system of claim 21 wherein said storage stores instructions that enable the processor to refrain from transferring the contents of the register back to the memory.

23. The system of claim 21 wherein said storage stores instructions that enable the processor to determine whether the register has been updated and if so, save the contents of the register to the memory.

24. The system of claim 23 wherein said storage stores instructions that enable the processor to save the register contents to memory on a context change.

25. The system of claim 19 including a storage to store said bit.

26. The system of claim 19 including a control register storing said bit and wherein said storage storing instructions and control register are part of said processor.

27. The system of claim 19 including a plurality of registers coupled to said processor and a single indicator bit for all of those registers.